A Simplified Microwave Model of the GaAs Dual-Gate MESFET

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Abstract — **A simplified wide-band model of the GaAs dual-gate MESFET based upon the familiar cascode representation is presented, which is valid over the frequency range of 2–11 GHz. The equivalent circuit contains 14 elements and the parameter values are directly determined from 3-port *S*-parameters over the frequency range of 4–6 GHz, and dc data. Separate microwave measurements of each FET part are not required, thus greatly reducing the number of measurements required to fully characterize the device. The method has been used to model a GaAs dual-gate MESFET in which both FET parts were in the saturation region, and good agreement has been obtained between measured and calculated results without the need for computer optimization.**

I. Introduction

THE DUAL-GATE GaAs MESFET has found application in a wide range of signal processing circuits. This is due to its inherent versatile functional capability as a device with two control gates, coupled with enhanced isolation characteristics. Circuit applications of dual-gate MESFET's include frequency converters and multipliers [1], [2], modulators [3], pulse regenerators [4], phase shifters [5], and variable gain amplifiers [6].

Being a four-terminal device, however, causes additional complexity in the modeling procedure, and this has hampered the design and analysis of dual-gate FET circuits. The basic device model is constructed from a cascode connection of two single-gate FET's. Initial modeling techniques utilized approximate analytical expressions to determine the element values in the equivalent circuit [7], [8]; however, this leads to limited accuracy and frequency range of validity, especially if the assumption of equal FET parts is made [9].

A more accurate modeling method has been reported recently by Tsironis and Meierer [10]. This utilizes dc and microwave measurements to characterize each FET part separately under its actual bias conditions. Though the method is quite general, it involves 28 circuit elements and requires several sequential steps for evaluation. At a given device bias point, two sets of two-port *S*-parameters need to be measured at two different auxiliary bias conditions, as well as the three-port *S*-parameters of the device over a broad frequency range. In addition, a total of four levels of computer optimization are required to define the model elements, making the entire procedure very lengthy. A refinement of this technique was reported by Ashoka and Tucker [11], although the method basically employed similar principles.

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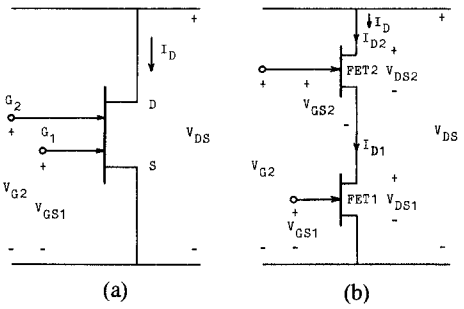

Fig. 1. (a) Dual-gate MESFET. (b) Decomposition into an equivalent cascode connection of two single-gate MESFET's.

The purpose of this paper is to present a new simple and efficient modeling procedure for the dual-gate MESFET. The active device model contains 14 elements and is derived from a design-oriented equivalent circuit developed previously for single-gate MESFET's [12]. The dual-gate FET characterization is extremely efficient and rapid since it only requires some dc data and three-port *S*-parameter measurements at a few frequencies, and utilizes simple analytical relations, yet the model applies with good accuracy over a wide frequency range.

The simplified device model is presented in Section II. Section III describes the parameter acquisition technique for determining the model elements, and relevant three-port parameter transformations are given in the Appendix. The model accuracy is evaluated in Section IV, which presents a comparison between predictions and measured microwave parameters on an actual dual-gate FET.

II. Simplified Circuit Model

The dual-gate MESFET representation as a cascode connection of two single-gate FET parts [3], [7], [8] is depicted in Fig. 1. The equivalent circuit is deduced by combining two single-gate FET models [7], [8], [10]; however, the resulting equivalent circuit tends to be too complex for design and for parameter acquisition.

In order to obtain a more tractable representation, a simplified model was established for the device, and efficient analytical techniques for parameter evaluation were developed. Previous work by one of the authors [12] has shown that the conventional single-gate FET model shown in Fig. 2(a) may be reduced to the simplified form of Fig. 2(b) with little loss of accuracy for frequencies up to

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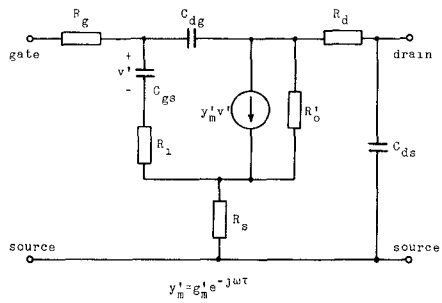
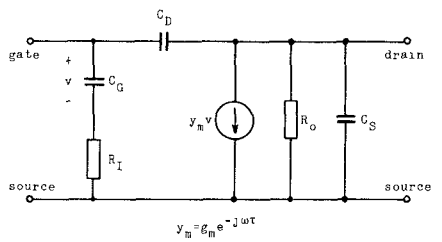


(a)



(b)

Fig. 2. Single-gate MESFET models. (a) Conventional model. (b) Simplified model (after Minasian [12]).

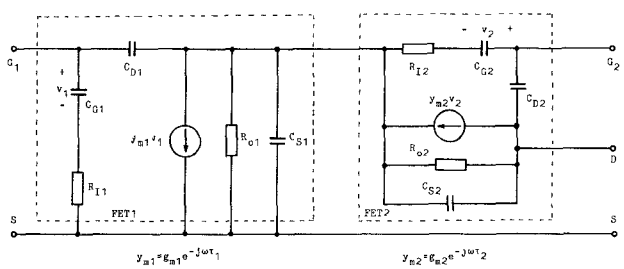


Fig. 3. Simplified dual-gate MESFET equivalent circuit.

12 GHz. The simplified circuit also has the advantage that all the element values may be determined directly from microwave measurements. The application of these constituent FET models to obtain a circuit model for the dual-gate FET is shown in Fig. 3, where the terminals refer to the active device terminals. The model contains 14 elements and represents a substantial simplification compared to previous dual-gate FET models.

To test the validity of the new simplified dual-gate MESFET model, three-port S-parameters referenced to the active device terminals were calculated over the frequency range of 2–11 GHz for the simplified model of Fig. 3 and the more detailed model of Tsironis and Meierer [10]. The element values for the full model were those of Tsironis and Meierer's FET(a), while the corresponding element values for the simplified model were derived from those of the full model using [12, eq. (14)–(19)]. It was found that the magnitudes of all the nine S-parameters were within 4 percent of those of the full model, and the phase discrepancy of all the S-parameters was less than 3 degrees over the entire 2–11-GHz range. This verifies the excellent accuracy of the dual-gate FET model of Fig. 3 compared to more detailed models, while at the same time enabling a substantially simplified representation.

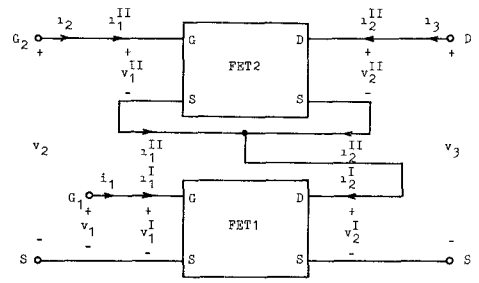


Fig. 4. Cascode connection of two two-port networks (FET1 and FET2) to form a three-port network.

III. Determination of Model Elements

One of the principal aims of the modeling procedure was to arrive at a rapid and efficient parameter acquisition technique. The analytical basis for the expressions used for element evaluation is now described.

A. FET1 Model Elements

If FET1 and FET2 are represented by their two-port z-parameters $[Z^{\mathrm{I}}]$ and $[Z^{\mathrm{II}}]$, respectively, the dual-gate MESFET may be represented as a cascode connection of two two-port networks as shown in Fig. 4, resulting in a three-port network, with port voltages and currents as defined in Fig. 4. Taking port 1 as being between gate 1 and the source, port 2 as being between gate 2 and the source, and port 3 as being between the drain and the source, the cascode connection forces the following relationships between the three-port terminal voltages and currents and the terminal voltages and currents on the constituent two-port networks (FET1 and FET2):

$$v_1 = v_1^{\mathrm{I}} \tag{1}$$

$$v_2 = v_2^{\mathrm{I}} + v_1^{\mathrm{II}} \tag{2}$$

$$v_3 = v_2^{\mathrm{I}} + v_2^{\mathrm{II}} \tag{3}$$

$$i_1 = i_1^{\mathrm{I}} \tag{4}$$

$$i_2 = i_1^{\mathrm{II}} \tag{5}$$

$$i_3 = i_2^{\mathrm{II}}. \tag{6}$$

Using (1)–(6), the following simple relationships may be found between the three-port z-parameters $[Z]$ of the dual-gate MESFET (which may be derived from measured three-port S-parameters using the transformation in Appendix I) and the individual two-port z-parameters of the two single-gate FET's:

$$\begin{aligned} Z_{11} &= Z_{11}^{\mathrm{I}} & Z_{12} &= Z_{12}^{\mathrm{I}} & Z_{13} &= Z_{12}^{\mathrm{I}} \\ Z_{21} &= Z_{21}^{\mathrm{I}} & Z_{22} &= \left(Z_{22}^{\mathrm{I}} + Z_{11}^{\mathrm{II}}\right) & Z_{23} &= \left(Z_{22}^{\mathrm{I}} + Z_{12}^{\mathrm{II}}\right) \\ Z_{31} &= Z_{21}^{\mathrm{I}} & Z_{32} &= \left(Z_{22}^{\mathrm{I}} + Z_{21}^{\mathrm{II}}\right) & Z_{33} &= \left(Z_{22}^{\mathrm{I}} + Z_{22}^{\mathrm{II}}\right). \end{aligned} \tag{7}$$

It can be seen readily from (7) that three of the four two-port z-parameters of FET1 (Z_{11}^{I}, Z_{12}^{I}, and Z_{21}^{I}) are given explicitly, and that the fourth parameter Z_{22}^{I} is added

to each of the four z-parameters of FET2. In order to complete the two-port description for FET1, an estimate of Z_{22}^{I} is required. An analysis of the z-parameter expressions for the single-gate FET model in Fig. 2(b) shows that up to moderate frequencies

$$Z_{12} \approx \frac{C_D}{C_G + C_D} Z_{22}.$$

This expression is accurate within 2-percent magnitude for frequencies to at least 6 GHz. Since $C_D \ll C_G$, this implies that $Z_{12} \ll Z_{22}$. Hence, assuming that $Z_{12}^{\mathrm{II}} \ll Z_{22}^{\mathrm{I}}$, then the estimate for Z_{22}^{I} can be formed from

$$Z_{22}^{\mathrm{I}} \approx Z_{23}. \tag{8}$$

Equation (8) has been found to give reasonable accuracy for the overall determination of FET1 elements, especially since the other three z-parameters are obtained explicitly from the matrix in (7).

Inspection of (7) also shows that two estimates are available for both Z_{12}^{I} and Z_{21}^{I}. Ideally, $Z_{21}^{\mathrm{I}} = Z_{21} = Z_{31}$ and $Z_{12}^{\mathrm{I}} = Z_{12} = Z_{13}$. In practice, the simplest means of accounting for errors in the measured three-port z-parameter data is to average the two available estimates; i.e., $Z_{21}^{\mathrm{I}} = (Z_{21} + Z_{31})/2$ and $Z_{12}^{\mathrm{I}} = (Z_{12} + Z_{13})/2$. A further improvement in accuracy is possible by choosing those relevant three-port z-parameters which are less sensitive to small errors in the measured S-parameters. Such a sensitivity analysis was carried out and indicated that $\mathrm{Re}(Z_{13})$, $\mathrm{Im}(Z_{12})$, and $\mathrm{Im}(Z_{21})$ were slightly more robust in their insensitivity to small errors in the measured S-parameters. Hence, the following expressions are likely to yield the most accurate values for Z_{12}^{I} and Z_{21}^{I}:

$$\mathrm{Re}(Z_{12}^{\mathrm{I}}) = \mathrm{Re}(Z_{13}) \tag{9}$$

$$\mathrm{Im}(Z_{12}^{\mathrm{I}}) = \mathrm{Im}(Z_{12}) \tag{10}$$

$$\mathrm{Re}(Z_{21}^{\mathrm{I}}) = (\mathrm{Re}(Z_{21}) + \mathrm{Re}(Z_{31}))/2 \tag{11}$$

$$\mathrm{Im}(Z_{21}^{\mathrm{I}}) = \mathrm{Im}(Z_{21}). \tag{12}$$

By using (7)–(12), the four z-parameters of FET1 may be determined directly from the three-port z-parameters of the dual-gate MESFET. The FET1 z-parameters $[Z^{\mathrm{I}}]$ may then be converted to y-parameters $[Y^{\mathrm{I}}]$ by a matrix inversion, and these y-parameters then are used to calculate the FET1 model elements using the expressions in [12]. For convenience, these expressions are reproduced in Appendix II.

B. FET2 Model Elements

A study of (7) shows that the two-port z-parameters of FET2 $[Z^{\mathrm{II}}]$ appear in the three-port z-parameters with Z_{22}^{I} added to them. Hence, errors in the Z_{22}^{I} estimate from the three-port z-parameters cause a systematic error to propagate in all of the $[Z^{\mathrm{II}}]$ elements. For example, the assumption that $Z_{22}^{\mathrm{I}} \approx Z_{23}$ means that the model for FET2 must be unilateral (since Z_{12}^{II} must be zero), which will degrade accuracy. Hence, a decomposition of the matrix in (7) to give $[Z^{\mathrm{II}}]$ using an estimate for Z_{22}^{I} could not be used in the case of FET2 for accuracy reasons.

Instead, expressions were developed to determine the FET2 element values from measured three-port y-parameters of the device, together with the already evaluated FET1 elements. The general expressions for the three-port y-parameters of the model in Fig. 3 were derived, and it was found that the remaining 7 elements of FET2 could be evaluated, provided an estimate for the transconductance of FET2 (g_{m2}) was available. This element may be determined quite simply from dc measurements using a new analytical dc model which has recently been published by one of the authors [13]. The method uses new closed-form expressions to calculate the internal voltages of the two single-gate FET parts from the external bias conditions on the complete dual-gate MESFET, and hence defines the operating state of each single-gate FET part. The transconductance of FET2 then may be determined using the following expression:

$$g_{m2} = \frac{\partial I_{D2}}{\partial V_{GS2}} \tag{13}$$

where I_{D2} and V_{GS2} are defined in Fig. 1(b).

The FET2 elements in terms of the FET1 elements g_{m2} and the three-port y-parameters may be obtained successively using the expressions presented below.

Assuming that

$$(1 + j\omega C_{G1} R_{\mathrm{I1}}) \approx 1 \tag{14}$$

and

$$(1 + j\omega C_{G2} R_{\mathrm{I2}}) \approx 1 \tag{15}$$

then

$$C_{G2} \approx \frac{1}{\omega} \mathrm{Im}\left[\frac{-g_{m2}}{1 + \dfrac{Y_{12}(y_{m1} - j\omega C_{D1})}{Y_{21}(j\omega C_{D1})}} \right] \tag{16}$$

$$g_{02} = \frac{1}{R_{02}} \approx -\omega C_{G2} \mathrm{Im}\left[\frac{Y_{31}}{Y_{21}} \right] - g_{m2} \tag{17}$$

$$C_{D2} \approx -\frac{\mathrm{Im}[Y_{23}]}{\omega} - \frac{C_{G2} g_{02}}{g_{m2} + g_{01} + g_{02}} \tag{18}$$

$$C_{S2} \approx \mathrm{Im}\left[\frac{-(Y_{23} + j\omega C_{D2})(y_{m1} - j\omega C_{D1})}{\omega Y_{21}} \right] \tag{19}$$

where

$$y_{m1} = g_{m1} e^{-j\omega\tau_1}.$$

Also, if

$$C_{G2} \gg g_{m2}\tau_2$$

then

$$\tau_2 \approx -\frac{1}{\omega}\left\{ \arg\left(\frac{Y_{31}}{Y_{21}} \right) + \frac{\pi}{2} \right\}. \tag{20}$$

It has been found that, for a range of typical dual-gate MESFET parameters, the above approximations are valid for frequencies up to at least 6 GHz. The final element R_{I2} was assumed to be equal to R_{I1}. This assumption does not

affect the accuracy of the model very much, as its effect on the calculated S-parameters is fairly small. The transformation from three-port S-parameters to three-port y-parameters is presented in Appendix I.

IV. Results

In order to test the performance of the present modeling procedure, measured three-port S-parameter data for a dual-gate MESFET as reported by Tsironis and Meierer [10] was used as a basis for comparison. The device (designated FET(a) in [10]) has gate 1 dimensions of 0.8×200 μm, gate 2 dimensions of 2×200 μm, an intergate spacing of 2 μm and is biased with both FET parts in the saturation region.

Before commencing the modeling, the S-parameters were de-embedded back through the mounting parasitics so as to be referenced to the active device terminals. This requires characterization of parasitic elements such as bond wire inductances and test circuit interelectrode capacitances which are dependent upon the particular device mounting configuration used. One of the more important elements is the parasitic feedback capacitance between the first gate and the drain, which has an adverse effect on transistor performance [7]. Since there is a screening effect of the second gate on the device, the main contribution to this interelectrode capacitance usually comes from the test fixture [7]. This capacitance is accounted for as part of the embedding network, though in order to ensure it has a small effect on the parameters, a mounting configuration with low stray interelectrode coupling is desirable.

For best accuracy, measured S-parameter data for element evaluation of the model was taken in the 4–6-GHz range. (At lower frequencies, the sensitivity of the z-parameter and y-parameter transformations to errors in measured S-parameters increases, while at higher frequencies the assumptions in the analytical expressions for the model elements degrade.)

The results for the model elements obtained for the dual-gate MESFET are presented in Table I. The g_{m2} value used was derived from the value given by Tsironis and Meierer using [12, eq. (16)] because accurate dc information on the device was not available. Only three measured S-parameter data points were needed at 4, 5, and 6 GHz. The FET1 values obtained from this data was averaged, and these averaged values then were used to calculate the FET2 element values, which were averaged in turn.

An error function defined by

$$\mathrm{EF}=\left\{\sum_{f_k}\sum_{i,j}\frac{|S_{ij}\mathrm{meas}-S_{ij}\mathrm{calc}|^2}{\sum_{f_k}\sum_{i,j}|S_{ij}\mathrm{meas}|^2}\right\}^{1/2},$$

$$k=1,\ldots 10,(i,j)=(1,2,3) \quad (21)$$

(as used in [10], for comparison purposes) was evaluated for the S-parameters calculated with the element values given in Table I. The value of the error function EF was

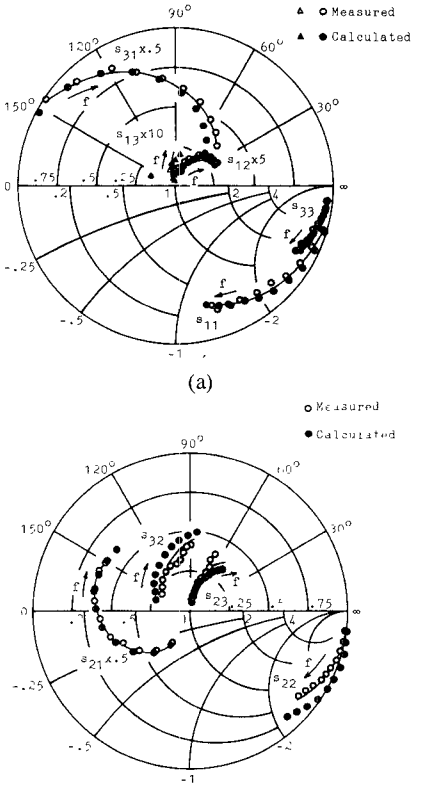


Fig. 5. Measured and calculated three-port S-parameters of the dual-gate MESFET with both FET parts in saturation. $V_{DS}=5$V, $V_{GS1}=-1$V, $V_{G2}=+2$V, $I_D=34$mA. Port 1 = gate 1, port 2 = gate 2, port 3 = drain. Frequency: 2–11 GHz, $\Delta F=1$ GHz.

TABLE I
Equivalent Circuit Element Values of the Dual-Gate MESFET ($i=1,2$)

Partial FET	C_{Di}	C_{Gi}	C_{Si}	R_{Oi}	R_{Ii}	g_{mi}	τ_i
FET 1	20fF	0.181pF	51fF	350Ω	17Ω	24.3mS	0.7ps
FET 2	17fF	0.288pF	48fF	400Ω	17Ω	15.0mS	5.6ps

9.8 percent over the frequency range of 2–11 GHz, which compares favorably with a value of EF ≈ 8 percent obtained using Tsironis and Meierer's equivalent circuit.

A plot of the measured and calculated three-port S-parameters of the dual-gate MESFET referenced to the active device terminals is given in Fig. 5(a) and (b). As expected from the value obtained for the error function, the agreement between the measured and calculated parameters is very good, although some small discrepancies do occur at the higher frequencies. These discrepancies may be due partially to the mounting parasitic element values used for de-embedding, or due to measurement errors arising from the microwave test fixture used [10] (eg., for S_{13} and S_{23}).

If desired, the overall model accuracy can be improved further by employing a computer optimization on the

simplified model to minimize the error function EF. Since the model contains only 14 elements, and since the error function value without any optimization is low (9.8 percent), optimization towards a global minimum should proceed readily.

V. Conclusions

A simplified model of the GaAs dual-gate MESFET has been developed where all of the parameters are determined from three-port S-parameter measurements over the 4–6 GHz frequency range, except for one transconductance element, which can be evaluated from dc data. The three-port S-parameters are measured with the transistor dc biased for normal operation, and no two-port S-parameter measurements under special bias conditions are required, which significantly reduces the number of RF measurements that need to be made. The method has been used to model a dual-gate MESFET where both FET parts are in saturation, and good agreement between measured and calculated S-parameters has been achieved over a multi-octave frequency range (2–11 GHz) without using computer optimization.

Due to its relative simplicity and ease of parameter acquisition, while maintaining good accuracy, the method should prove useful in circuit design and in the study of element value variation with dc bias, for large-signal modeling of the dual-gate MESFET.

VI. Acknowledgment

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Appendix I

The following transformations for an n-port have been taken from [14]:

$$Z = Z_0(I+S)(I-S)^{-1} \tag{AI1}$$

$$S = (Z - Z_0 I)(Z + Z_0 I)^{-1} \tag{AI2}$$

$$Y = \frac{1}{Z_0}(I-S)(I+S)^{-1} \tag{AI3}$$

$$S = (I - Z_0 Y)(I + Z_0 Y)^{-1} \tag{AI4}$$

where

- S network S-parameters,
- I identity (unit) matrix,
- Z network z-parameters,
- Y network y-parameters, and
- Z_0 characteristic impedance (normally 50Ω).

Appendix II

The following expressions are reproduced from [12] for convenience, and applied to FET1.

Assuming $(\omega R_{I1} C_{G1})^2 \ll 1$:

$$C_{D1} = \frac{-\mathrm{Im}(Y_{12}^{\mathrm{I}})}{\omega} \tag{AII1}$$

$$C_{S1} = \frac{\mathrm{Im}(Y_{22}^{\mathrm{I}})}{\omega} - C_{D1} \tag{AII2}$$

$$R_{01} = \frac{1}{\mathrm{Re}(Y_{22}^{\mathrm{I}})} \tag{AII3}$$

$$g_{m1} = \mathrm{Re}(Y_{21}^{\mathrm{I}}) \tag{AII4}$$

$$C_{G1} = \frac{\mathrm{Im}(Y_{11}^{\mathrm{I}})}{\omega} - C_{D1} \tag{AII5}$$

$$R_{I1} = \frac{\mathrm{Re}(Y_{11}^{\mathrm{I}})}{(\omega C_{G1})^2} \tag{AII6}$$

$$\tau_1 = \left\{ -\frac{\mathrm{Im}(Y_{21}^{\mathrm{I}})}{\omega} - g_{m1} R_{I1} C_{G1} - C_{D1} \right\} / g_{m1}. \tag{AII7}$$

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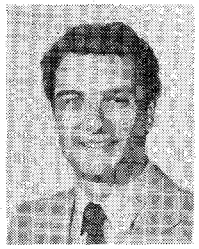

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Dual-Gate MESFET Mixers

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Abstract—**A theoretical and experimental investigation of dual-gate MESFET mixers is presented. Based on a detailed analysis of the different nonlinear modes of DGFET's, a computer-aided modeling procedure has been developed, which allowed to recognize and optimize critical circuit and bias conditions for high conversion gain and IF bandwidth. Theoretical results are in good agreement with experiments on a 12-GHz TV reception mixer with 8-dB conversion gain and 800-MHz bandwidth.**

I. INTRODUCTION

IN MODERN MICROWAVE superheterodyne receivers, GaAs FET's are used as preamplifiers, local oscillators, and mixers in hybrid [1] or monolithic [2] versions. Both single-gate FET's (SGFET's) and dual-gate FET's (DGFET's) are used as mixers, the last ones even up to *Ka*-band frequencies [3]. The advantages of employing DGFET's as down converters instead of Schottky diodes or SGFET's are, except for conversion gain and reasonable noise figure which are inherent also to SGFET mixers, the intrinsic separation of signal and local oscillator ports and the possibility of separate matching and direct combination of the corresponding powers inside the device. This avoids cumbersome passive couplers and is an important requirement of monolithic circuit designs. The MMIC's DGFET mixers are probably the only adequate solution, as has been shown in the case of *X*-band direct satellite broadcasting receivers [2].

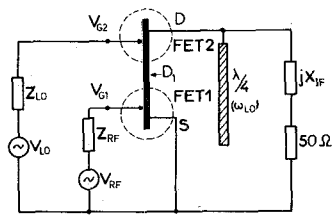

Fig. 1. Principle of DGFET mixer operation.

In spite of the obvious importance of the mixer application of DGFET's, the mixing mechanism of this device is not yet completely understood. This is due to the floating potential of the intergate channel region (D_1 in Fig. 1) strongly dependent on the amplitude of the local oscillator voltage applied onto either of the two gates. The bias and saturation conditions of both FET parts of the DGFET are consequently changing during LO voltage excursion and cause them to act as a mixer, or as RF resp. IF amplifier separately.

This paper deals with computer-aided modeling optimization and testing of DGFET mixers in the three principal mixing modes of practical interest. After an initial general investigation of mixing possibilities with DGFET's, the modeling procedure is described, and examples for two

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